In the Claims:

Please cancel claims 7, 12, 13 and 17 and replace them with new claims 18, 19, 20 and 21. This listing replaces all prior versions.

1. (Currently Amended) A microcontroller architecture comprising: a processor ~~(101)~~ for processing of instruction data comprising memory access instructions for accessing of a memory circuit, the processor operating responsive to a clock circuit for providing clock cycles~~(105)~~; at least a pointer memory circuit ~~(103a, 103b, 103c, 103d)~~ for storing of a pointer address forming part of the instruction data; at least a pointer register ~~(200a, 200b, 200c, 200d)~~ for storing a duplicate of the pointer address; ~~and,~~ a control circuit ~~(102)~~ for determining whether one of a read operation from the at least a pointer memory circuit ~~(103a, 103b, 103c, 103d)~~ and a write operation to the at least a pointer memory circuit ~~(103a, 103b, 103c, 103d)~~ is to take place; wherein the clock circuit is coupled to the at least a memory circuit, the at least a pointer register and the control block, and the read operation accesses a region in the memory circuit that is addressed by the target pointer address within a single clock cycle of determining a read operation is to take place, and wherein for a write operation the control circuit ~~(102)~~ stores the pointer address in the at least a pointer memory circuit ~~(103a, 103b, 103c, 103d)~~ and automatically stores a duplicate in the at least a pointer register ~~(200a, 200b, 200c, 200d)~~ and where for a read operation the control circuit utilizes the at least a pointer register ~~(200a, 200b, 200c, 200d)~~ to access data pointed to by a target pointer address derived from the pointer address stored therein ~~and other than~~ without accessing[es] the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~.

2. (Currently Amended) A microcontroller architecture according to claim 1, comprising a pointer multiplexer block ~~(300)~~ having at least an input port coupled to the at least a pointer register ~~(200a, 200b, 200c, 200d)~~ for receiving a pointer address and an output port for providing the pointer target address used for indirect addressing operations of data stored within the memory circuit ~~(105)~~.

3. (Currently Amended) A microcontroller architecture according to claim 2, comprising a source select block ~~(600)~~ having a first input port for receiving a next program address derived from a current program counter value plus a length of a current instruction, a second input port for receiving the pointer target address from the pointer multiplexer block ~~(300)~~, a third input port for receiving a selection signal from the control circuit ~~(102)~~ for determining which data bits from the at least one of the input signals received at the first and second input ports are to be used for providing of pointer data output signals from output ports of the source select block ~~(600)~~.

4. (Currently Amended) A microcontroller architecture according to claim 3, wherein the at least a pointer register ~~(200a, 200b, 200c, 200d)~~ comprises a plurality of pointer registers ~~(200a, 200b, 200c, 200d)~~, the microcontroller architecture comprising an input multiplexer ~~(400)~~ having input ports coupled to the output ports of the source select block ~~(600)~~ for receiving of the pointer data output signals therefrom, and for receiving of an input data multiplexer control signal from the control block ~~(102)~~, the input multiplexer control signal for determining which data bits derived from the pointer data output signals are to be used in forming of the pointer address for storage in the plurality of pointer registers ~~(200a, 200b, 200c, 200d)~~.

5. (Currently Amended) A microcontroller architecture according to claim 4, wherein the at least a pointer memory circuit ~~(103a, 103b, 103c, 103d)~~ comprises a plurality of pointer memory circuits ~~(103a, 103b, 103c, 103d)~~, the microcontroller architecture comprising an output multiplexer ~~(500)~~ having input ports coupled to plurality of pointer memory circuits ~~(103a, 103b, 103c, 103d)~~ for receiving of data bits derived from the stored pointer address stored within the plurality of pointer memory circuits ~~(103a, 103b, 103c, 103d)~~ and having an output port for providing a program counter value for being restored during a return from interrupt instruction.

6. (Currently Amended) A microcontroller architecture according to claim 5, wherein the pointer multiplexer ~~(300)~~ and the output multiplexer ~~(500)~~ and the input multiplexer ~~(400)~~ are ~~other than~~ not clock circuit gated.

7. (Cancelled)

8. (Currently Amended) For use with a processor responsive to clock cycles, a[~~A~~] method of pointer based addressing comprising the steps of: providing at least a pointer memory ~~(103a, 103b, 103c, 103d)~~; providing at least a pointer register ~~(200a, 200b, 200c, 200d)~~; storing of a pointer address data in the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~; ~~and,~~ upon storing ~~(701)~~ of a pointer address data in the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~, automatically storing a duplicate pointer address data, which is a duplicate of the pointer address data, in the at least a pointer register; receiving ~~(702)~~ a memory access request to a memory location within a memory for retrieving of data stored at the memory location addressed by the pointer address; retrieving the duplicate pointer address data from the pointer register; and, accessing the memory using a target pointer address derived from the duplicate pointer address data without using a target pointer address derived from the pointer address data stored in the at least a pointer memory, wherein the steps of retrieving and accessing occur within one clock cycle of the step of receiving. ~~(200a, 200b, 200c, 200d)~~.

9. (Original) A method according to claim 8, wherein the step of automatically storing is performed within a same clock cycle as the step of storing.

10. (Currently Amended) A method according to claim 8, wherein the step of automatically storing is performed after the step of storing such that the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~ is ~~other than~~ not accessible by other operations until the step of automatically storing is completed.

11. (Currently Amended) A method according to claim 8 comprising the step of detecting all changes to the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~ for automatically storing the duplicate pointer address data.

12. (Cancelled)

13. (Cancelled)

14. (Currently Amended) A method according to claim 8 ~~12~~, comprising the step of writing back the target pointer address to the at least a pointer register ~~(200a, 200b, 200c, 200d)~~ and to the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~.

15. (Currently Amended) A method according to claim 8 ~~12~~, comprising the step of detecting all changes to the at least a pointer memory ~~(103a, 103b, 103c, 103d)~~ for automatically storing the duplicate pointer address data.

16. (Currently Amended) A method according to claim 8 ~~12~~, wherein the at least a pointer register ~~(200a, 200b, 200c, 200d)~~ comprises a plurality of pointer registers ~~(200a, 200b, 200c, 200d)~~, wherein the step of accessing comprises the step of multiplexing of the pointer address data stored in the plurality of pointer registers ~~(200a, 200b, 200c, 200d)~~ to form the target pointer address for accessing of the random access memory ~~(105)~~.

17. (Cancelled)

18. (New) For use with a microcontroller, an arrangement for pointer based addressing of a first block of memory, the arrangement comprising:

a first plurality of pointer registers containing data corresponding to locations in the first block of memory;

a second plurality of pointer registers that contain duplicate data corresponding to data stored in said locations in the first block of memory;

a second block of memory that is accessible independently from the first block of memory and that stores data corresponding to data stored at the locations in the first block of memory;

a first multiplexer that selectively provides a first multiplexer output that is one of data from the plurality of pointer registers and a data corresponding to a next program address;

a second multiplexer that selectively provides a second multiplexer output that is one of a low, middle and high data portion from the first multiplexer output, the second multiplexer output providing data to said first plurality of pointer registers and to said second plurality of pointer registers;

an third multiplexer that selectively provides a third multiplexer output that includes portions of data from said second plurality of pointer registers, the third multiplexer output providing data to said first block of memory for addressing purposes;

a fourth multiplexer that selectively provides a fourth multiplexer output that includes portions of data from the second multiplexer output and portions of data from the second block of memory; and

a control logic block that is responsive to the microcontroller and that provides control signals to the first plurality of pointer registers, the second plurality of pointer registers, the second block of memory, the first multiplexer, the second multiplexer, the third multiplexer and the fourth multiplexer.

19. (New) The arrangement of claim 18, wherein the first block of memory provides data to the microcontroller within on clock cycle of the microcontroller decoding an instruction indicating a pointer-read operation.

20. (New) The arrangement of claim 18, wherein the control logic block receives an end of instruction flag from the microcontroller.

21. (New) The arrangement of claim 18, wherein second multiplexer output is arranged to selectively provide data from an arithmetic logic unit (ALU).